Remarks

This is in response to the final Office Action mailed on January 14, 2004. Claims 1 and 6 have been amended, support for the amendments being found, for example, at Figure 4 and page 5, lines 14-18 of the present application. Claims 1-6 remain pending. Reconsideration and allowance are respectfully requested.

Claims 1 and 6 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the rejection states that the recitation "in combination" does not seem to be supported. This rejection is respectfully traversed, and the correctness of the rejection is not conceded.

Claims 1 and 6 recite a power supply capacitor cell corresponding to a logic gate cell. This configuration is illustrated, for example, at Figure 4 of the present application. Claims 1 and 6 are fully supported by the application. Reconsideration and allowance are respectfully requested.

Claims 1, 3, 4, and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kinoshita, U.S. Patent No. 5,869,852, in view of Young, U.S. Patent No. 6,229,861. This rejection is respectfully traversed, to the extent it is maintained.

Claim 1 recites, among other limitations, that the capacitance value of a power supply capacitor cell is determined based on the drive load capacity value of a logic gate cell. Claim 1 further recites arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.

The rejection concedes that Kinoshita fails to disclose or suggest that a capacitance value of the power supply capacitor cell is determined based on a drive load capacity value of the logic gate cell, as recited by claim 1.

Further, Kinoshita discloses a feed through cell that is used as a bypass capacitor. See Kinoshita, column 3, line 63 - column 4, line 4. Therefore, Kinoshita also fails to disclose or suggest arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell, as recited by claim 1.

Young discloses matching of the interconnect capacitance of a logic gate to achieve an evenly balanced delay. See Young, column 4, lines 44-59. The interconnect capacitance corresponds to a load capacitance of DCS 30. Young, column 4, lines 26-34. The capacitances of capacitors C_B, C_{CL1}, C_{CL2}, C_{CL2}, etc. disclosed in Young do not indicate drive load capacity.

Therefore, Young fails to disclose or suggest that the capacitance value of a power supply capacitor cell is determined based on the drive load capacity value of a logic gate cell which is used to determine the capacitance value, as recited by claim 1. Young also fails to disclose or suggest arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell, as recited by claim 1.

For at least these reasons, neither Kinoshita nor Young, alone or in combination, disclose an LSI layout method including a capacitance value of a capacitor cell that is determined based on a drive load capacity value of the logic gate cell, that the capacitor cell that is disposed between a power supply line and a ground line, and that the capacitor cell is arranged in a vicinity of the logic gate cell, as recited by claim 1. Reconsideration and allowance of claim 1, as well as claims 3 and 4 that depend therefrom, are respectfully requested.

Claim 6 is similar to claim 1, except that claim 6 recites that the power supply capacitor cell is arranged adjacent to the logic gate cell. For similar reasons to those noted above with respect to claim 1, neither Kinoshita nor Young render claim 6 obvious under section 103(a). Reconsideration and allowance are respectfully requested.

Claim 5 was rejected under section 103(a) as being unpatentable over Kinoshita in view of Young and further in view of Kusunoki et al., U.S. Patent No. 5,512,766. In addition, claim 2 was rejected under section 103(a) as being unpatentable over Kinoshita in view of Young and further in view of Mihara et al., U.S. Patent No. 5,406,510. These rejections are respectfully traversed, and the correctness of the rejections is not conceded.

However, claims 2 and 5 both depend from claim 1. Neither Kusunoki nor Mihara, alone or in combination, remedy the shortcomings of Kinoshita and Young noted above. Therefore, claims 2 and 5 should be allowable for at least the same reasons as those provided above with respect to claim 1. Reconsideration and allowance are respectfully requested.

In view of the above, favorable reconsideration of claims 1-6 in the form of a Notice of Allowance is requested. The Examiner is invited to contact the undersigned at (612) 371-5237 with any questions regarding this application.

Respectfully submitted,
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